

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a timer circuit configured to present any of a plurality of divided delay signals as a wake-up signal in response to an input signal and an enable signal; and

5 a microcontroller configured (i) to exit a suspend or sleep mode in response to said wake-up signal and (ii) to generate said input signal and said enable signal, wherein (i) said input signal comprises a programmable delay value ~~determined by~~ and (ii) said microcontroller is configured to determine said programmable
10 delay value during an awake mode in response by (a) initially setting said programmable delay value to a predetermine
predetermined delay value, (b) starting said timer circuit, (c) measuring a delay time between enabling said timer circuit and
assertion of said wake-up signal and (d) adjusting said
15 programmable delay value based on said measured delay time.

2. (ORIGINAL) The apparatus according to claim 1, wherein said input signal comprises a user programmable signal.

3. (ORIGINAL) The apparatus according to claim 1, wherein said input signal comprises a multi-bit signal.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said programmable delay value is determined by said microcontroller in response to one or more firmware instructions.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said programmable delay value comprises a wake-up delay timing value.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said timer circuit comprises:

a delay circuit configured to generate a delay signal;
and

5 a select circuit configured to (i) generate said plurality of divided delay signals and (ii) present said wake-up signal in response to said delay signal and said input signal.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said input signal is configured to control selection of one of said plurality of divided delay signals for presentation as said wake-up signal.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein each of said divided delay signals has a period that comprises a multiple of a period of said delay signal.

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said select circuit is configured to multiplex said plurality of divided delay signals in response to said input signal.

10. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said select circuit comprises:

a divider circuit configured to generate said plurality of divided delay signals in response to said delay signal; and

5 a multiplexer configured to present said wake-up signal in response to said plurality of divided delay signals and said input signal.

11. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~first~~ timer circuit comprises a counter configured to generate each of said plurality of divided delay signals in response to a different value of said input signal.

12. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said delay circuit is further configured to present said delay signal in response to said enable signal.

13. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said input signal is generated in response to a value stored in a register of said microcontroller.

14. (CURRENTLY AMENDED) An integrated circuit comprising:

a controller configured (i) to operate in a sleep mode and a wake-up mode and (ii) to generate an enable signal and an adjust signal, wherein said controller is configured to determine said adjust signal is determined in response during said wake-up mode by (a) initially setting said adjust signal to a predetermined delay value, (b) starting a timer circuit, (c) measuring a delay time between enabling said timer circuit and a wake-up signal during said wake-up mode and (d) changing said adjust signal based on said measured delay time; and

a said timer circuit configured to control switching of said controller from said sleep mode to said wake-up mode after a programmable period of time, wherein said timer circuit comprises (i) a delay block configured to generate a delay signal in response to said enable signal and (ii) a divider circuit configured to

generate a plurality of divided delay signals in response to said delay signal, where said plurality of divided delay signals determine a range of said programmable period of time and said timer circuit is configured to select one of said plurality of delay signals as said wake-up signal in response to said adjust signal.

15. (CURRENTLY AMENDED) A method for adjusting wake-up timing comprising the steps of:

(A) receiving an input signal and an enable signal from a microcontroller;

(B) generating a delay signal in response to said enable signal;

(C) generating a wake-up signal by dividing said delay signal according to a value of said input signal; and

(D) waking-up said microcontroller in response to said wake-up signal, wherein (i) said input signal comprises a programmable delay value ~~determined by~~ and (ii) said microcontroller is configured to determine said programmable delay value during an awake mode in response by (a) initially setting said programmable delay value to a predetermine predetermined delay value, (b) enabling generation of said wake-up signal, (c) measuring a delay time between enabling generation of said wake-up

signal and assertion of said wake-up signal and (d) adjusting said programmable delay value based on said measured delay time.

16. (PREVIOUSLY PRESENTED) The method according to claim 15, wherein said input signal comprises a user programmable signal and said programmable delay value comprises a wake-up timing value.

17. (PREVIOUSLY PRESENTED) The method according to claim 15, wherein said programmable delay value is determined in response to execution of one or more computer executable instructions stored in a computer readable medium.

18. (PREVIOUSLY PRESENTED) The method according to claim 15, further comprising the steps of:

generating a plurality of divided delay signals in response to said delay signal; and

5 selecting one of said divided delay signals as said wake-up signal in response to said programmable delay value.

19. (PREVIOUSLY PRESENTED) The method according to claim 15, wherein step (C) further comprises the sub-step of:

programming a counter in response to said programmable delay value and clocking said counter in response to said delay signal.

20. (CURRENTLY AMENDED) The method according to claim 15, further comprising the step of:

repeating said adjustment of adjusting said value of said input signal ~~in response to a comparison of a measured wake-up delay to said predetermined delay value~~ to account for changes in operating conditions.

21. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said timer circuit and said microcontroller are implemented on a single integrated circuit.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein (i) said timer circuit is configured to periodically wake up said microcontroller and (ii) a sleep period of said microcontroller is determined by said programmable delay value.

23. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said microcontroller is further configured to repeatedly adjust said programmable delay value of said input signal in response to a comparison between ~~a~~ said predetermined ~~wake-up time~~ delay value and ~~a~~ a subsequently measured ~~wake-up~~ delay time.

24. (CURRENTLY AMENDED) The method according to claim 15, wherein said microcontroller is further configured to repeat the steps comprising:

setting said programmable delay value to said
5 predetermined delay value;

~~enabling a wake-up delay timer configured to generate~~
generation of said wake-up signal in response to said programmable
delay value;

measuring ~~a~~ said delay time between enabling generation
10 of said wake-up ~~timer~~ signal and assertion of said wake-up signal;
and

adjusting said programmable delay value in response to a
result of comparing said measured delay time with a predetermined
wake-up delay time corresponding to said predetermined delay value.

25. (PREVIOUSLY PRESENTED) The integrated circuit
according to claim 14, wherein said controller is configured to
determine a value for said adjust signal that produces said
programmable period of time.